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**Connect up the circuit below using Multisim (or CircuitLab if Multisim is not working) placing**

**the voltmeters at the locations shown. Set the Process Transconductance (KP) to 0.02 (this is**

**done by double clicking on the transistor giving you a menu on the right of the screen).**

**You should use the NMOS 4T from the menu of components. Remember to connect the**

**substrate to the Source.**

***(i) Run the simulation. What do you observe? Please provide a superimposed plot***

***of the node voltages using Grapher. [10 Marks]***

**My circuit:**

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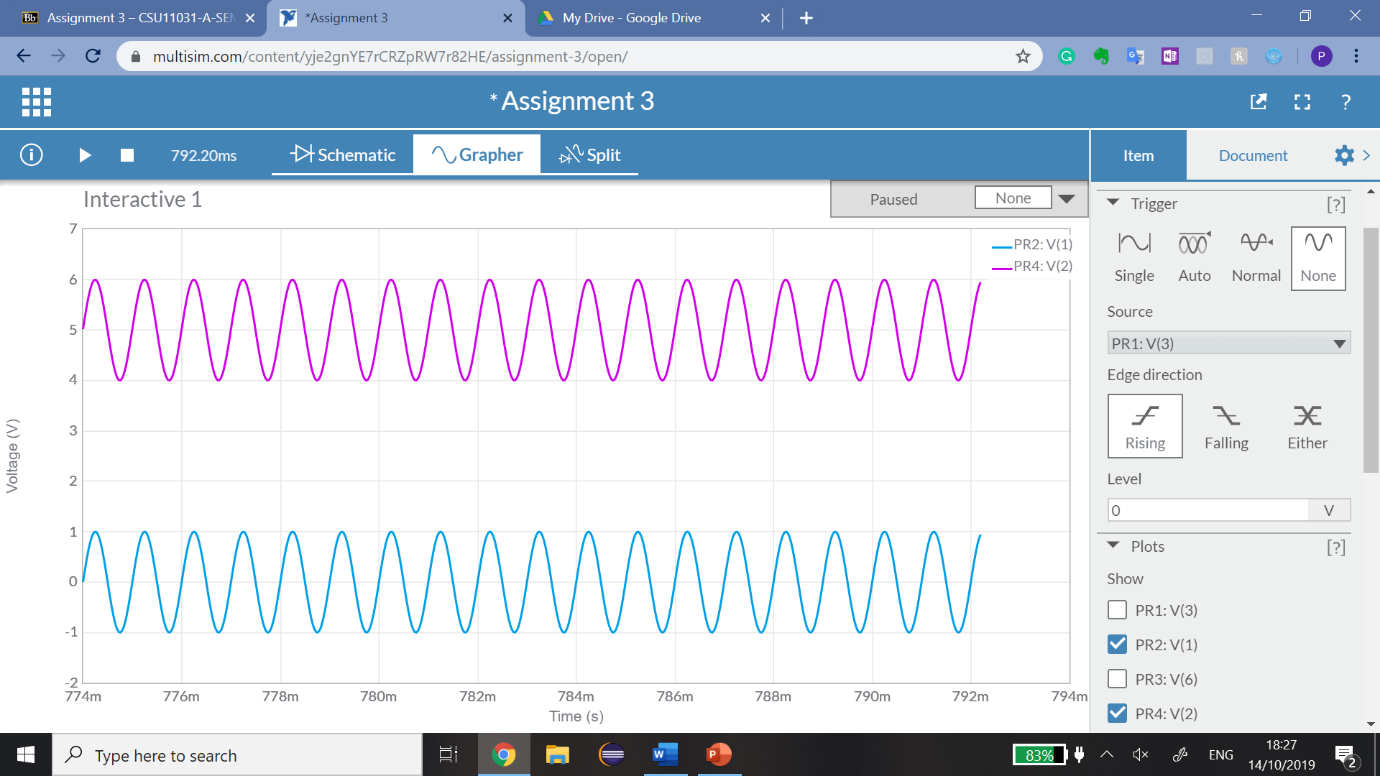
**My Graph:**

***A screenshot of a computer

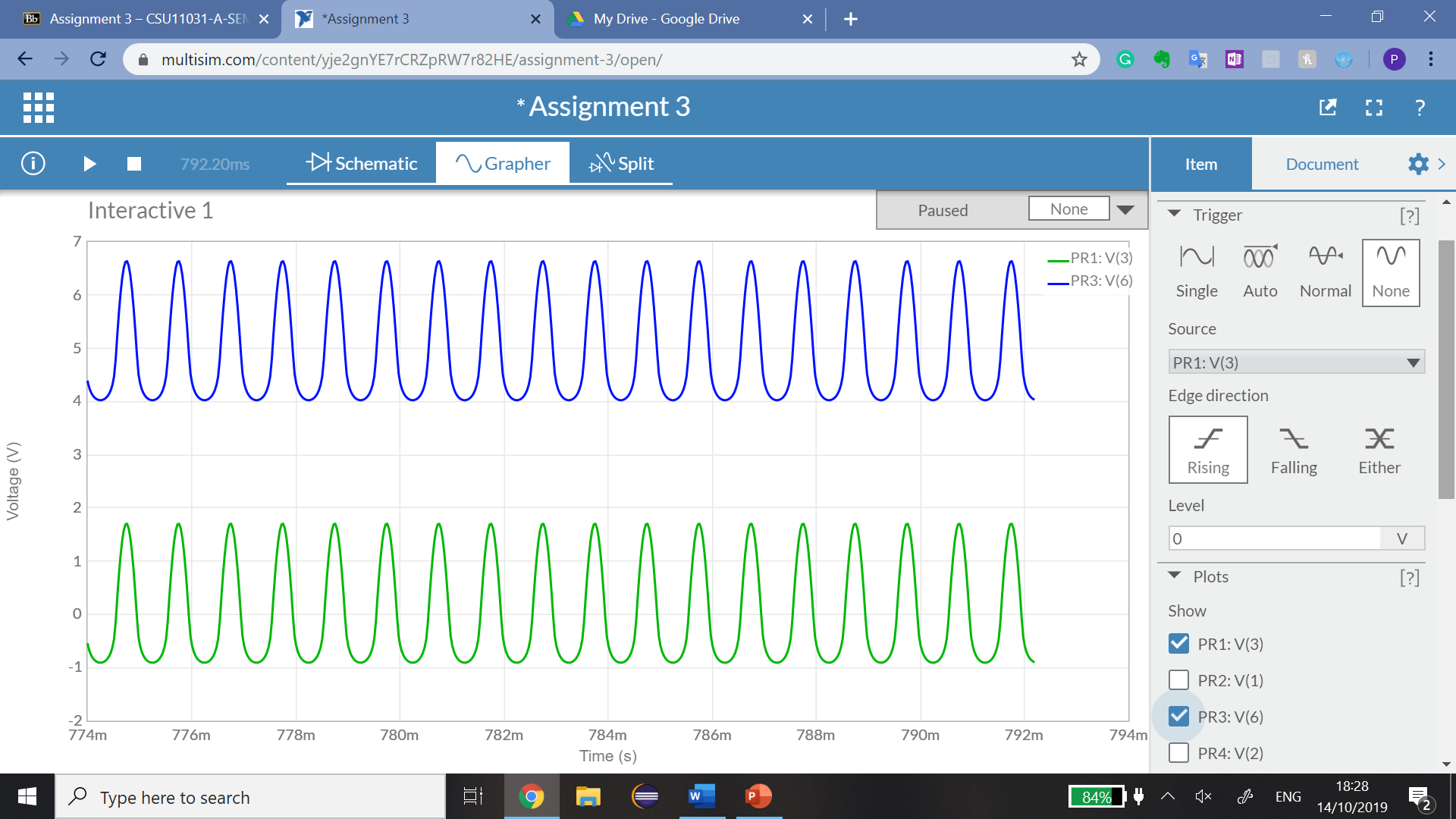
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**My Observations:**

* The voltages of PR2 and PR4 (the light blue and purple coloured lines on the plot) have cosine graphs
* The voltage range of PR4 (Purple line) is 4.0030V -> 5.9970V.
* The voltage range of PR2 (Light blue line) is -998.49mV -> 998.49 mV.

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* However, the voltages PR1 and PR3 have a variant of a sinusoidal graph.
* The voltage range of PR3(Dark Blue line) is 4.0254V -> 6.5352V
* The voltage range of PR1(Green line) is -909.08mV -> 1.7025V



***(ii) Calculate the voltage at the gate of the transistor. Does your answer tally with***

***the result given in Grapher? [10 Marks]***

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| Macintosh HD:Users:eamonnonuallain:Downloads:tran55.gif |  |

**In this case,**

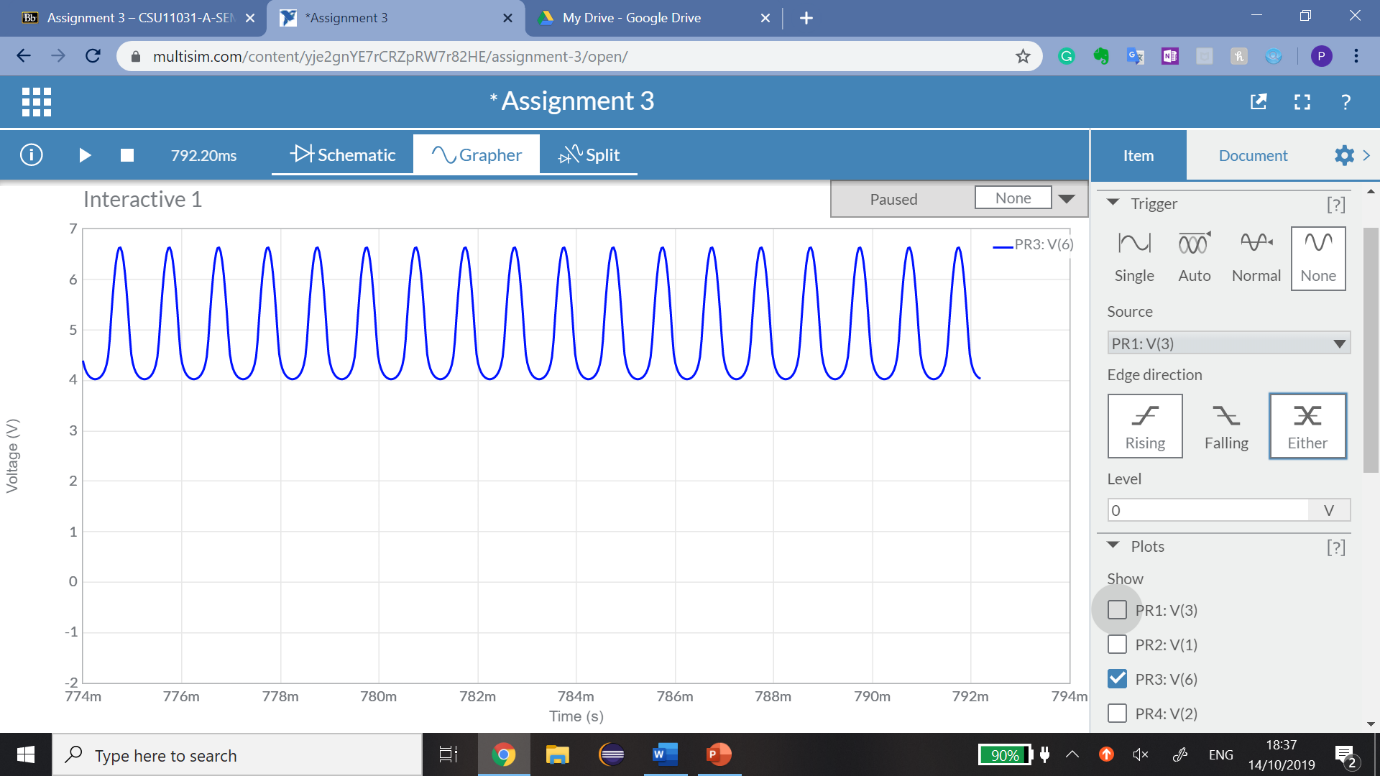
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* On Grapher, the voltage is in the range of 4.0030V -> 5.9970V, and our calculated value of 5V is between the range indicated by Grapher on Multisim.
* Because it’s an AC source, the voltage changes with respect to time.
* However, our calculated value is between the range indicated on Multisim. (i.e 5V is between 4.0030V and 5.9970V.

***(iii) Observe the Drain voltage in Grapher. Explain why it has an A.C. and D.C.***

***component. [20 Marks]***

* There are three parts to a NMOS transistor. The gate, the source, and the drain. The drain voltage can be identified from PR3; the voltmeter. The graph of PR3 is as follows:

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* The drain voltage changes with time, hence it is a function of time.
* The range of the drain voltage varies from is 4.0254V to 6.5352V.

**Why it has an A.C component:**

* The drain voltage has an A.C component because the voltage varies with time as shown in the graph above. The alternate current reverses direction many times a second, so the voltage changes with respect to time. This is illustrated in our plot.
* Since the voltage varies with time, this trait is reflected in PR3. This means PR3 (representing the drain voltage) has an A.C component.

**Why it also has a D.C component:**

* Since the voltage range of PR3 (representing the drain voltage) is not negative (i.e from 4.0254V to 6.5352V.), there is no backwards current in PR3.
* Since there is no backwards current in PR3, it’s coming from a D.C supply.
* There is also a constant voltage in the circuit from the D.C supply; there is a high voltage in PR3 (peaks at 6.5352V) as opposed to the A.C supply voltage of 1V.
* This means the D.C supply (15V) plays a part in the voltmeter PR3 indicating that the drain voltage also has properties of direct current.
* The potential divider formed by 200k Ω and resistors provide a D.C gate voltage in excess of (i.e the minimum threshold voltage for the transistor to turn on).
* **This ensures that the transistor is turned on even for negative values for the in the input voltage caused by the A.C supply.**
* The input voltage at the gate is the ac input signal and the dc biasing voltage combined. Hence, the signal at the gate is an ac signal with a dc component.

**Hence, traits of both A.C and D.C are reflected in PR3, the drain voltage.**

**(iv) Explain the purpose of the capacitors at the input and the output. [10 Marks]**

* The capacitor and at the output and input respectively allow the ac signal through the circuit while stopping the DC to the source.
* This allows the AC component through the circuit, but it prevents the DC component.
* Hence, the capacitor interferes with the dc-bias of the circuit.
* The capacitor values are arranged such that they include very little reactance at the frequencies of operation. In this case, it is 0.12μF for the capacitor values for C1 and C2.

**(v) You will observe that the output voltage is inverted with respect to the input**

**voltage. Explain why this is so. [20 Marks]**

* In our case, when the voltage flows through the NMOS 4T in Multisim, the voltage is appropriately inverted based on the Input.
* A high input is turned into a low input and vice versa.
* The s (input voltage) is sinusoidal. Hence, electrons in the source and drain are alternating between attract and repel continuously.
* Therefore, a voltage is also applied across the drain and source, this voltage is also alternating between attract and repel.
* If s (input voltage) increases, the voltage-drop across the drain resistance () increases, therefore decreases.
* The relationship displayed here is inversely proportional, hence they are both 180° out of phase with each other.
* Since they are out of phase, the output voltage is inverted with respect to the input voltage.

***(vi) Estimate the gain of this amplifier? [10 Marks]***

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G =

Hence, the gain of this amplifier is:

G = -1.705074663